


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	24NOV23	D.BOISER
B	ECR-119026	07FEB24	D.BOISER

HOLE TOLERANCE				
UNLESS SPECIFIED				
PLATED: +/- .003				
NON PLATED: +/- .002				
FINISHED HOLES IN MILS				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	PLATED	QTY	TOLERANCE/NOTES
+	10.0	PLATED	932	DIA MAX
□	35.0	PLATED	16	
○	40.0	PLATED	20	
◇	63.0	PLATED	4	
△	100.0	PLATED	8	
□	213.0	PLATED	4	
A	125.0	NON-PLATED	4	
B	127.0	NON-PLATED	4	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		APPROVAL		DATE		 ANALOG DEVICES AHEAD OF WHAT'S POSSIBLE™		GLOBAL OPERATIONS & TECHNOLOGY 804 WOBURN STREET WILMINGTON, MA 01887	
		TOLERANCES							
		DECIMALS FRACTIONS ANGLES							
		.XX .010 .1/32 .1° 2°							
.XXX .005		MATERIAL		TITLE		FABRICATION LT4275B and LT8306 25.5W POE CLASS 2			
.XXXX .0050		TEST ENGINEER N/A		N/A					
		COMPONENT ENGINEER ADGT LIBRARY		24NOV23					
		TEST PROCESS N/A		N/A					
		HARDWARE RELEASE C. LAPPAY		07FEB24					
FINISH		PCB DESIGNER C. LAPPAY		07FEB24		SIZE	FSCM NO	DRAWING NUMBER	REV
		ENGINEER D. BOISER		07FEB24		D	24355	09-081007	B
		CHECKER N/A		N/A					
DO NOT SCALE DWG						SCALE	1/1		SHEET 1 OF 2

NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES (EXCEPT WHERE NOTED).
ALL DOCUMENTS & SPECIFICATIONS REFERRED TO BELOW SHOULD BE THE LATEST REVISIONS.

MATERIAL : HOMOGENOUS MATERIALS IN THIS BOARD SHALL BE COMPLAINT WITH THE EU DIRECTIVE 2002/95/EC

2. BOARD MATERIAL:(USE CHECKED ITEMS)
 (X) ISOLA 370HR OR EQUIVALENT
 () ISOLA-FR408HR OR EQUIVALENT
 () ISOLA IS410
 () MEGTRON 6
 () NELCO-4000-13
 () ROGERS 4350B
 () ROGERS 3003
 () ARLON 85N
 () EM370D
 () OTHER _____
3. ALL LAMINATES & BONDING MATERIALS SHOULD BE SELECTED FROM IPC-4101 OR IPC-4103.(TG>170 DEGC TD>300 DEGC)
 UL FLAMMABILITY RATING 94V-0. BOARD MATERIAL & CONSTRUCTION SHALL MEET THE REQUIREMENTS OF UL796/UL796F.
4. REFER TO IPC-6010 SERIES, CLASS 2 FOR FABRICATION.WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2.
5. REFER TO LAMINATION DIAGRAM FOR OVERALL BOARD THICKNESS. TOLERANCE APPLIES AFTER ALL LAMINATION AND PLATING
 PROCESSES. FINISHED THICKNESS MEASURED FROM TOP COPPER TO BOTTOM COPPER.
6. BOW & TWIST NOT TO EXCEED 0.0075 INCHES (0.75%) PER LINEAR INCH AND SHOULD BE MEASURED PER IPC-TM-650, METHOD 2.4.22.
7. ACCEPTABILITY PER ADI SPECIFICATION TST00115.

TOOLING :

8. IMPEDANCE REQUIREMENTS: IF NO STACKUP IS DEFINED, THE VENDOR IS ALLOWED TO ADJUST THE DIELECTRIC THICKNESS & TRACE WIDTHS TO MEET THE IMPEDANCE REQUIREMENT. IF SPECIFIED, THE VENDOR MUST MEET THE REQUIREMENTS LISTED IN THE IMPEDANCE TABLE. ANY ADJUSTMENT MADE TO THE DEFINED STACKUP, TRACE WIDTH & SPACING THAT IMPACT THE REQUIREMENTS MUST HAVE WRITTEN APPROVAL FROM ADI.
9. FILLET OPTIONS TO ENHANCE RELIABILITY AT PAD JUNCTIONS WHERE SPACING PERMITS.
() FILLETS ALLOWED
(X) FILLETS NOT ALLOWED
10. THIEVING:
() VENDOR MAY ADD THIEVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS MAINTAINING A MINIMUM 0.100 INCH CLEARANCE FROM ALL COPPER FEATURES.
() VENDOR MAY NOT ADD THIEVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS.
11. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.003 INCHES.

FINISH:


12. DRILL SIZES ARE FINISHED HOLE SIZES. ALL HOLES SHALL BE LOCATED WITHIN 0.005 INCHES DTP, MINIMUM BARREL PLATING OF 0.001 INCHES. PLATED HOLES SHALL NOT BE ROUGH OR IRREGULAR SO AS TO HINDER PROPER SOLDER WICKING. BARREL RELIEF ON SOLDERMASK ALLOWED IN UNFILLED VIA IN PAD HOLES.
13. PLATING SPECIFICATION:
(X) REFER TO LAMINATION DIAGRAM FOR FINISHED COPPER WEIGHT/THICKNESS REQUIREMENTS
THE STARTING COPPER WEIGHT/THICKNESS CAN VARY AS LONG AS THE FINISHED COPPER WEIGHT/THICKNESS IS NOT LESS THAN THE SPECIFIED VALUE.
14. SURFACE FINISH:
(X) IMMERSION GOLD (ENIG) 1.58-3.94 MICRO INCHES OVER 118-236 MICRO INCHES MIN. OF ELECTROLESS NICKEL PER IPC-452
() OSP (ORGANIC SOLDERABILITY PRESERVATIVE)
() IMMERSION SILVER
() SOFT WIRE BONDABLE GOLD 30-50 MICRO INCHES OF SOFT WIRE
BONDABLE GOLD OVER 100-150 MICRO INCHES OF NICKEL
() EDGE CONNECTOR FINGERS ARE TO BE PLATED WITH 100 MICRO-INCHES(.0001") OF LOW STRESS NICKEL UNDER 30 MICRO-INCHES (.0003") OF GOLD
() OTHER_____
15. SOLDERMASK:
SOLDERMASK OVER BARE COPPER OR BARE GOLD (BOTH SIDES) TO MEET IPC-SM-840.
IF PRESENT,DO NOT MODIFY SOLDERMASK DEFINED PADS (MASK OPENINGS LESS THAN COPPER PAD) WITHOUT APPROVAL.
(X) LPI
() OTHER_____
- COLOR
(X) GREEN
() OTHER_____
16. APPLY SILKSCREEN TO BOTH SIDES USING A NON-CONDUCTIVE, EPOXY BASED INK PER ARTWORK.
(X) WHITE
() OTHER


TESTING:

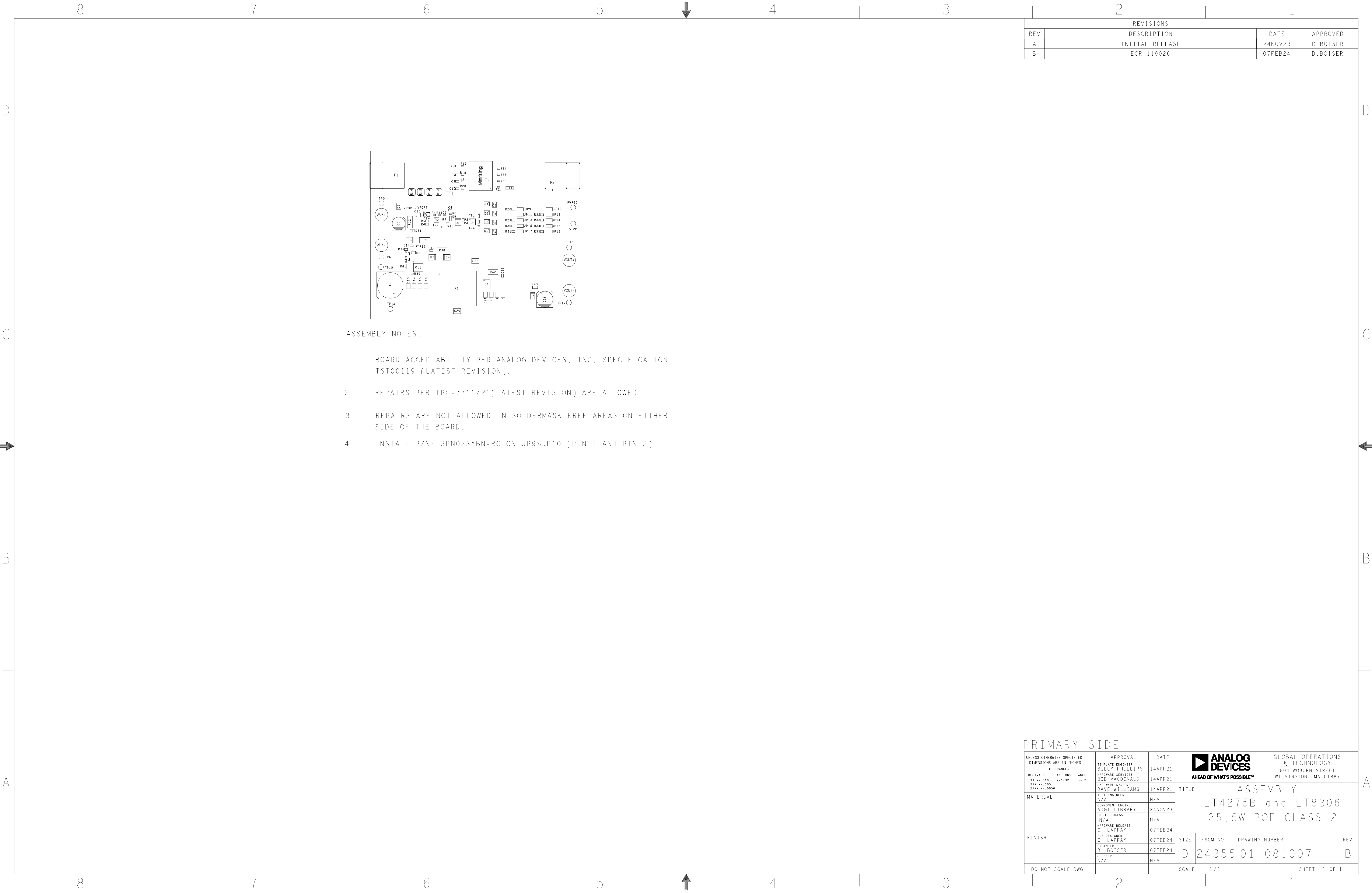
17. FINAL ELECTRICAL TESTS TO BE PERFORMED USING PROVIDED IPC-356A NETLIST OR ODB++ FORMAT FILE.
THE PCB SHALL HAVE A VERIFICATION STAMP.
 18. A TIME DOMAIN REFLECTOMETER REPORT (TDR) FOR EACH IMPEDANCE CONTROLLED LAYER & A CERTIFICATE OF COMPLIANCE SHALL BE PROVIDED BY VENDOR AT TIME OF SHIPMENT. INSTANCES WHERE TDR TESTING CAN'T BE PERFORMED BECAUSE THE TRACE LENGTH IS TOO SHORT ON THE OUTER LAYERS AT THE PIN ESCAPES IS ACCEPTABLE, ALL OTHER INSTANCES MUST BE REPORTED.
- MISCELLANEOUS:
19. IF PRESENT, ALL BLIND/BURIED VIAS WITH AN ASPECT RATIO <1:1 TO BE PLATED SHUT WITH COPPER WHEN USED AS VIA-IN-PAD OR AS A STACKED VIA. BLIND/BURIED VIAS WITH AN ASPECT RATIO >1:1 TO BE FILLED WITH NON-CONDUCTIVE EPOXY.
 20. FOR VIA FILL INFORMATION REFER TO DRILL CHART:
() NON-CONDUCTIVE EPOXY FILL ALL 0.XXXX INCHES DRILLED VIAS
() COPPER FILL ALL 0.XXXX INCHES DRILLED VIAS
 21. INTENTIONAL SHORTS:
IF AN INTENTIONAL SHORT REPORT IS SUPPLIED AND DOES NOT MATCH THE FAB DATA THEN ADI APPROVAL IS REQUIRED.
 22. PEMNUTS:
() PEMNUTS TO BE INSTALLED BY FABRICATOR
() PEMNUTS NOT TO BE INSTALLED BY FABRICATOR
() NOT APPLICABLE
 23. MANUFACTURER TO ETCH/STAMP WITH PERMANENT NON-CONDUCTIVE INK ON SECONDARY SIDE UNLESS OTHERWISE SPECIFIED:
A. UL CODE-FLAMMABILITY RATING FOR THOSE APPROVED MATERIALS(IF APPLICABLE)
B. DATE CODE
C. LOT NUMBER
D. MANUFACTURER LOGO
 24. PANELIZATION:
BOARDS TO BE SHIPPED IN SINGULATED AFTER FABRICATION PROCESS
SMOOTH EDGES AND FREE FROM BURRS AFTER DEPANELIZATION

25. MINIMUM DESIGN LINE WIDTH IS 0.008 INCH.
26. MINIMUM DESIGN LINE SPACING IS 0.00759 INCH.

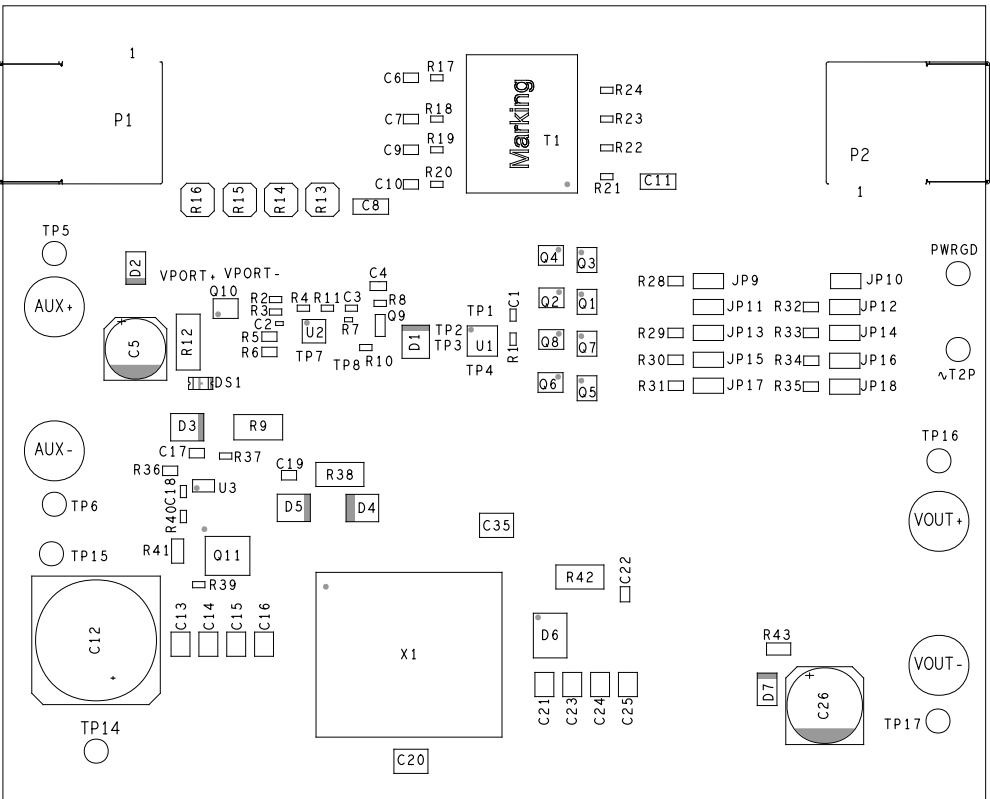
FAB NOTES REVISION: 2ND NOVEMBER 2022

LAMINATION DIAGRAM					
LAYER NUMBER	LAYER NAME	FINISHED CU WEIGHT (OZ)	DIELECTRIC THICKNESS (INCH)	MATERIALS	
1	TOP	2		FINAL CU THICKNESS AFTER PLATING	
2	L2_GND	1		TBD	ISOLA 370HR/EQUIVALENT
3	L3_PWR	1		TBD	ISOLA 370HR/EQUIVALENT
4	BOTTOM	2		TBD	ISOLA 370HR/EQUIVALENT
					FINAL CU THICKNESS AFTER PLATING
THE FINISHED PCB THICKNESS TO BE: 0.062" +/-10%					

 ANALOG DEVICES AHEAD OF WHAT'S POSSIBLE™		GLOBAL OPERATIONS & TECHNOLOGY 804 WOBURN STREET WILMINGTON, MA 01887	
SIZE	FSCM NO	DRAWING NUMBER	REV
D	24355	09-081007	B
SCALE	1/1		SHEET 2 OF 2




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A	INITIAL RELEASE	24NOV23	D.BOISER
B	ECR-119026	07FEB24	D.BOISER



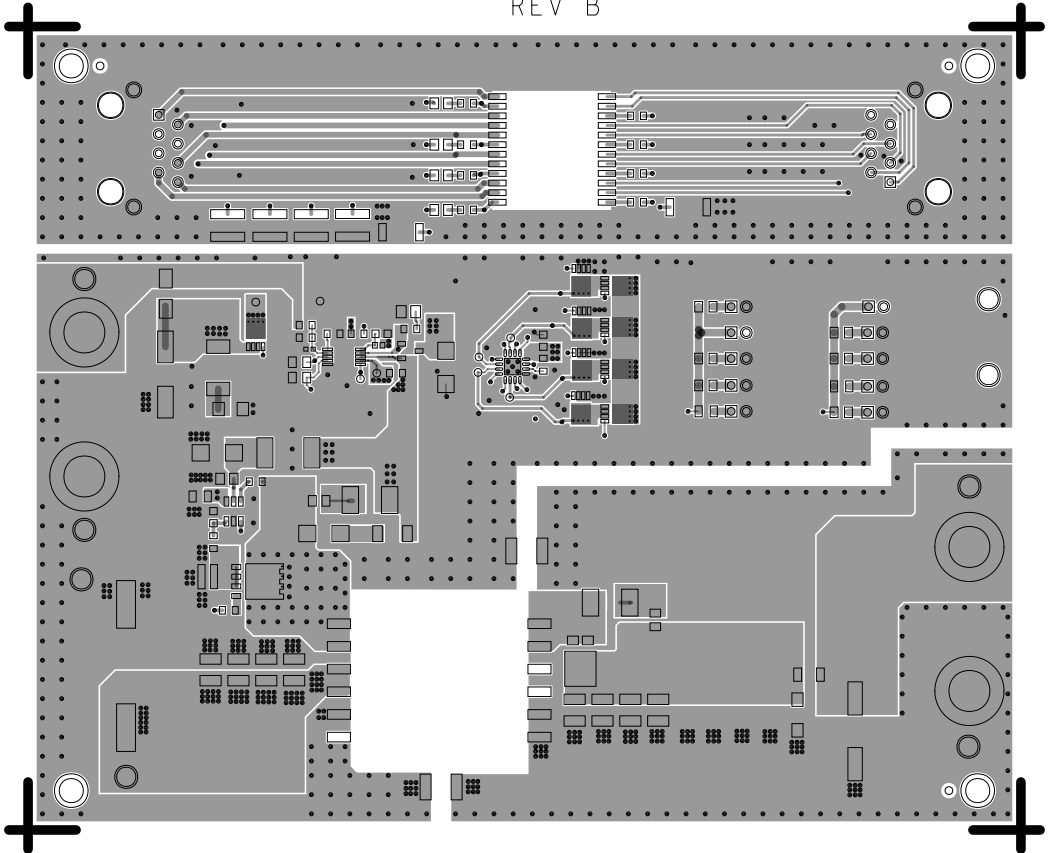
ASSEMBLY NOTES:

- BOARD ACCEPTABILITY PER ANALOG DEVICES, INC. SPECIFICATION TST00119 (LATEST REVISION).
- REPAIRS PER IPC-7711/21(LATEST REVISION) ARE ALLOWED.
- REPAIRS ARE NOT ALLOWED IN SOLDERMASK FREE AREAS ON EITHER SIDE OF THE BOARD.
- INSTALL P/N: SPN02SYBN-RC ON JP9~JP10 (PIN 1 AND PIN 2)

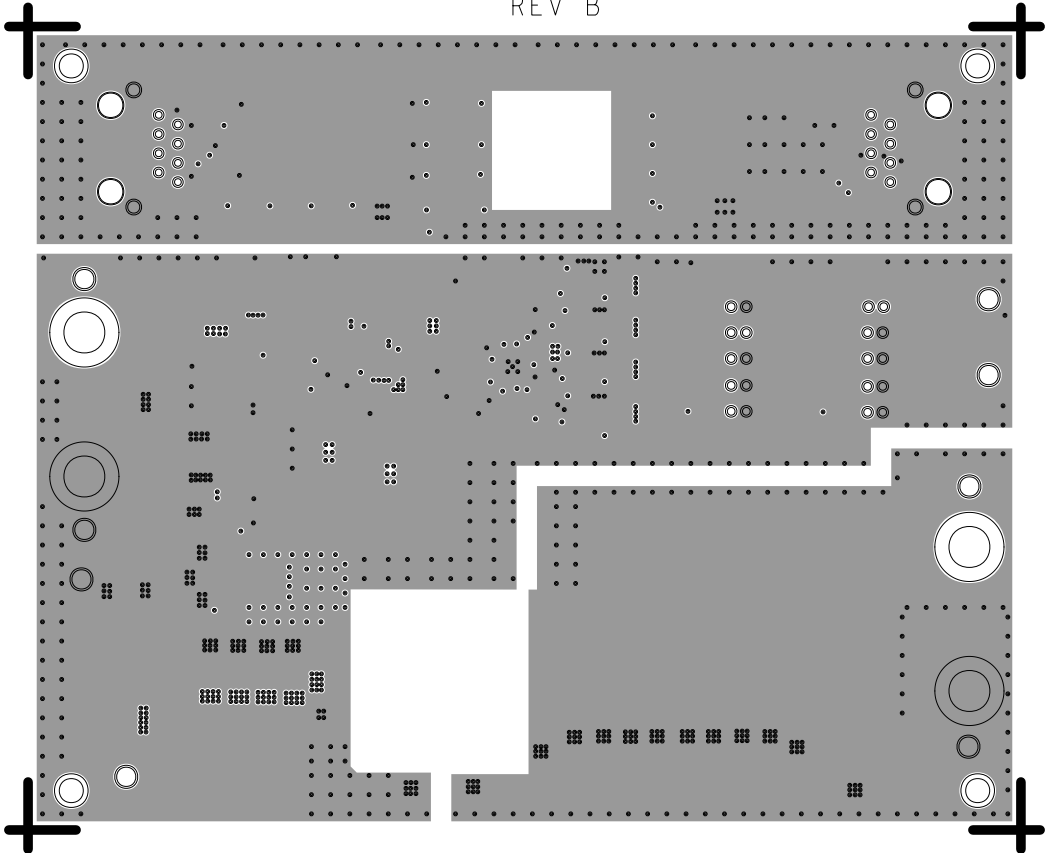
PRIMARY SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES .XX . . .010 . . .1/32 . . .2 .XXX . . .005XXXX . . .0050			APPROVAL		DATE		 GLOBAL OPERATIONS & TECHNOLOGY 804 WOBURN STREET WILMINGTON, MA 01887							
			TEMPLATE ENGINEER BILLY PHILLIPS		14APR21									
MATERIAL			HARDWARE SERVICES BOB MACDONALD		14APR21		TITLE ASSEMBLY LT4275B and LT8306 25.5W POE CLASS 2							
			HARDWARE SYSTEMS DAVE WILLIAMS		14APR21									
			TEST ENGINEER N/A		N/A									
			COMPONENT ENGINEER ADGT LIBRARY		24NOV23									
			TEST PROCESS N/A		N/A									
FINISH			HARDWARE RELEASE C. LAPPAY		07FEB24		SIZE D		FSCM NO 24355		DRAWING NUMBER 01-081007		REV B	
			PCB DESIGNER C. LAPPAY		07FEB24									
			ENGINEER D. BOISER		07FEB24									
			CHECKER N/A		N/A									
			DO NOT SCALE DWG											
			SCALE		1/1				SHEET		1 OF 1			

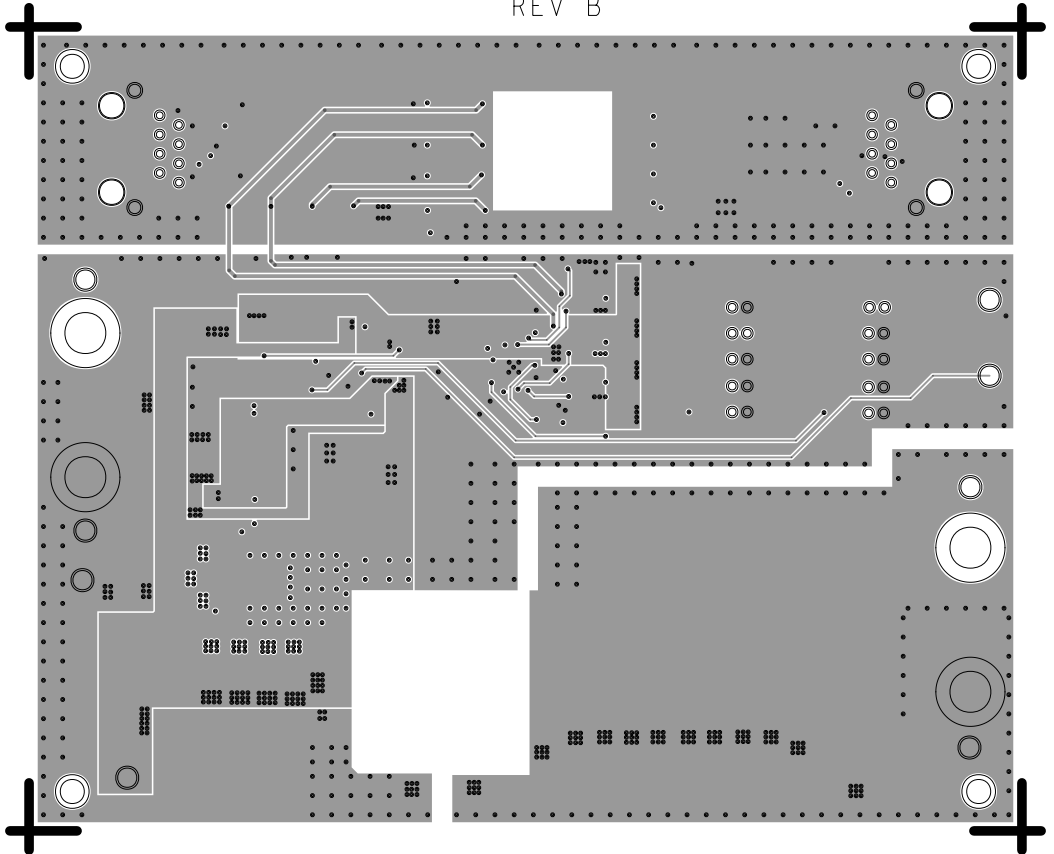
L1 PRIMARY
08-081007-01
REV B



L2 GND
08-081007-06
REV B



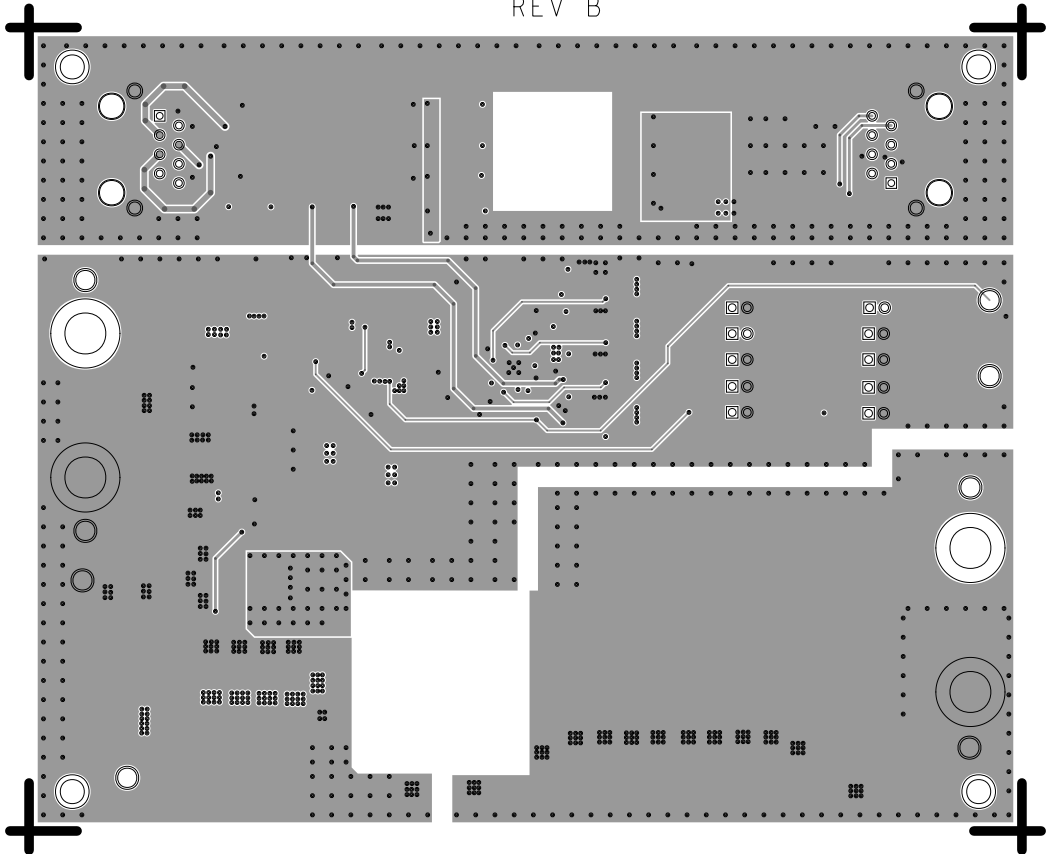
L3 PWR
08-081007-07
REV B



L4 SECONDARY

08-081007-02

REV B



SILKSCREEN PRIMARY

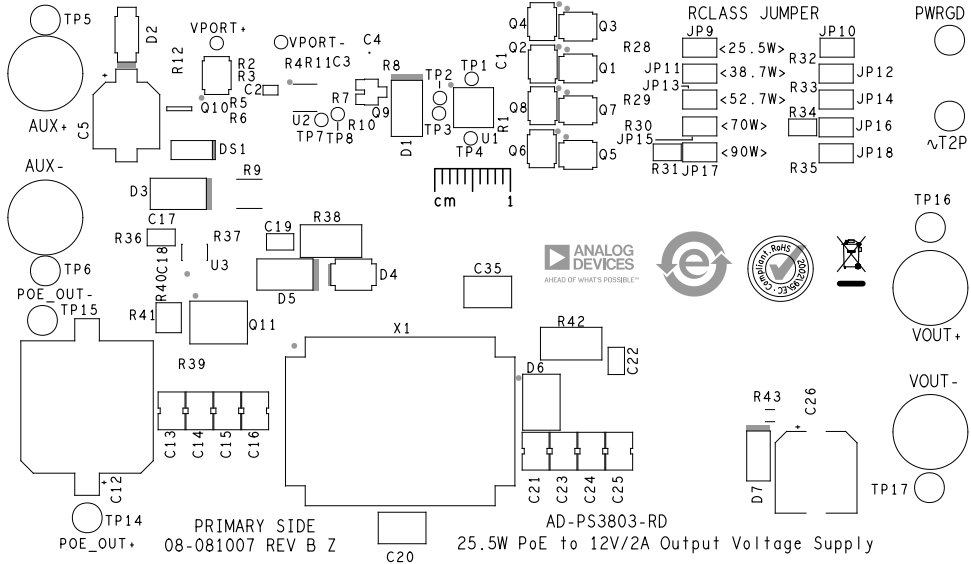
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REV B

IN FROM PSE, 37V-57V

ETHERNET INTERFACE

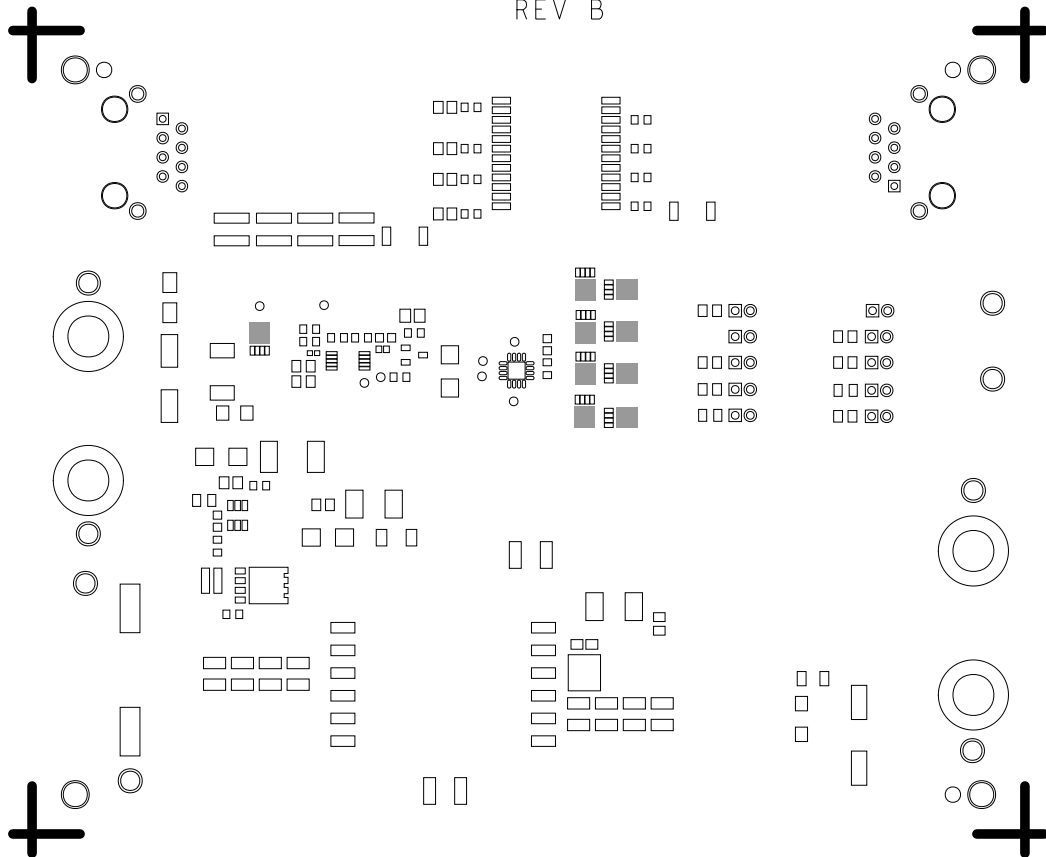
OUT TO PHY



SOLDERMASK PRIMARY

08-081007-04

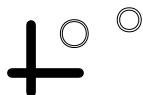
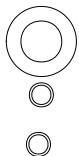
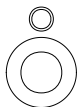
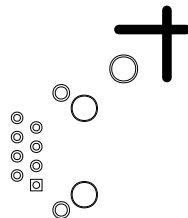
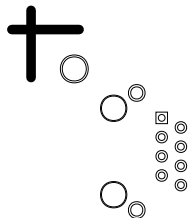
REV B



SOLDERMASK SECONDARY

08-081007-05

REV B



PASTEMASK PRIMARY

08-081007-08

REV B

